



SHAPING THE NEXT GENERATION OF ELECTRONICS

JUNE 23-27, 2024

MOSCONE WEST CENTER
SAN FRANCISCO, CA, USA





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Arteris - Accelerating Timing Closure for Network on Chip (NoCs) With Physical Awareness

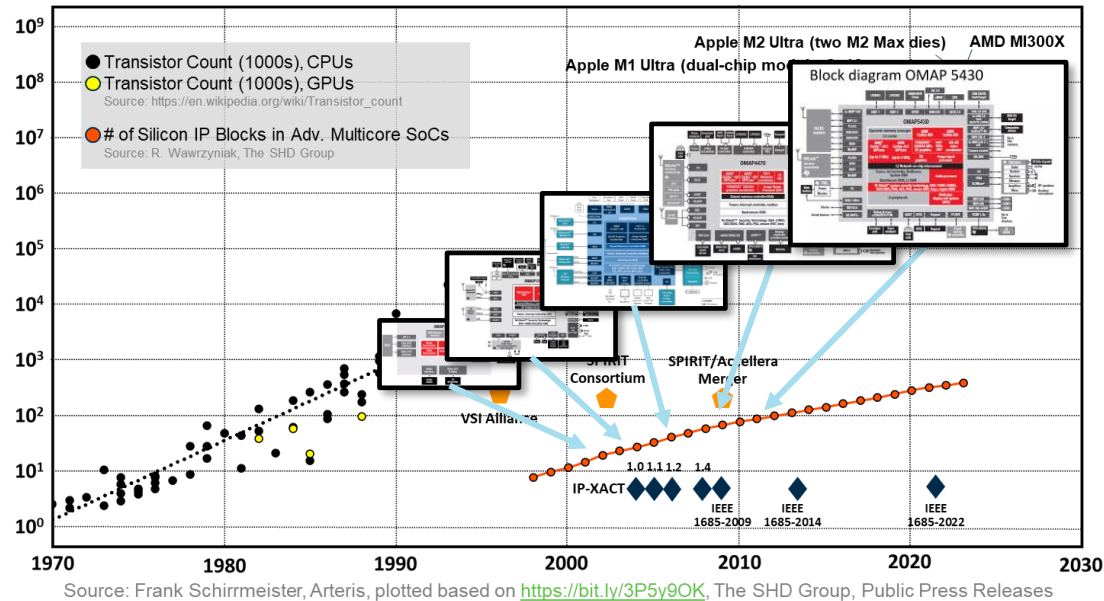
Andy Nightingale, Andy.Nightingale@arteris.com

Guillaume Boillet, Guillaume.Boillet@arteris.com



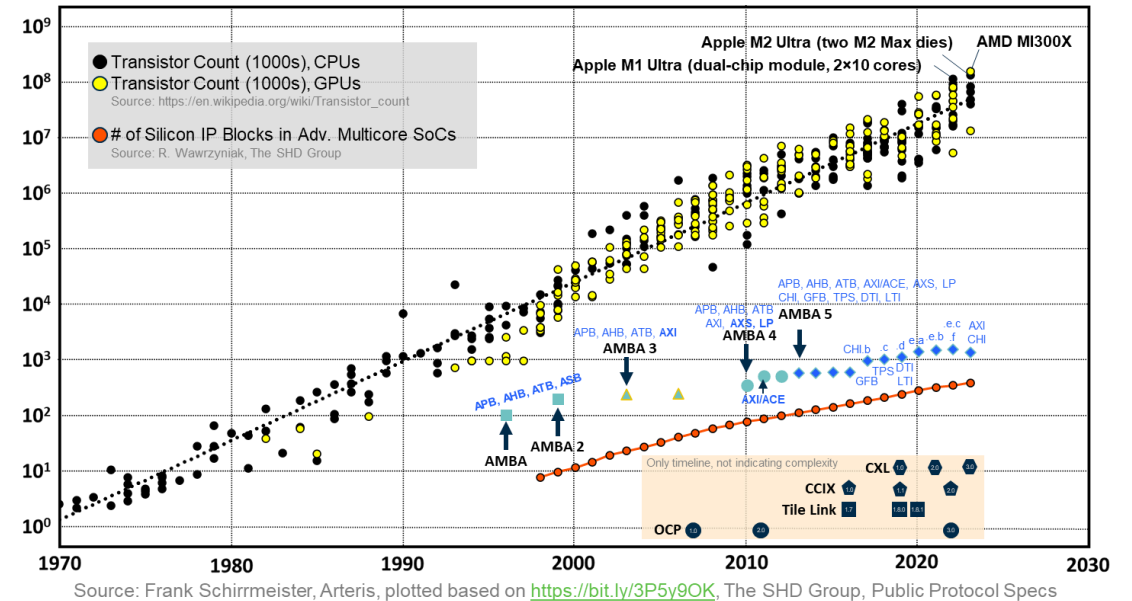
Semiconductor Complexity Continues to Grow Exponentially

Growing SoC Integration Complexity



- # of IP Blocks in SoC has grown from 10s to 100s
- Disaggregation offers design version variety
- Standards like IP-XACT need to extend too

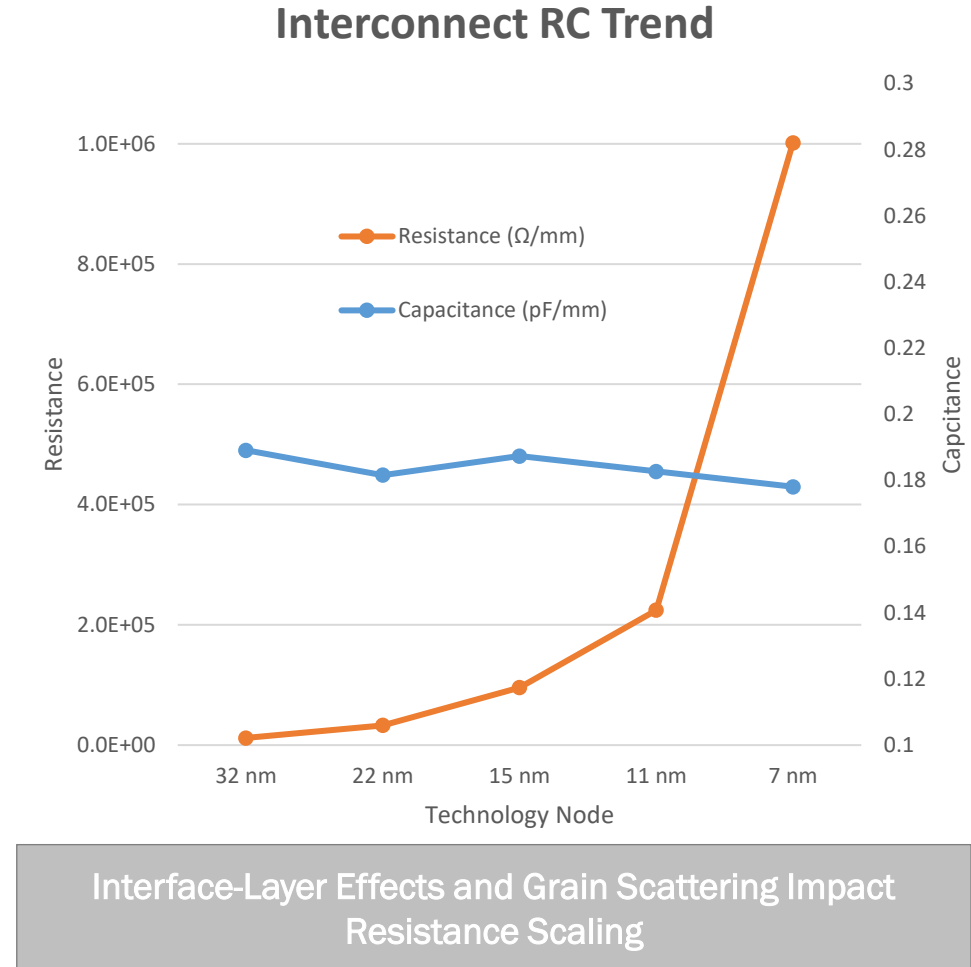
Growing Network-on-Chip Complexity



- Complexity of NoC protocols have grown 10x (# of pages)
- Variety of NoC protocols has grown
- NoCs evolve into Super-NoCs when split across chiplets

Physical Implementation is Hard to Predict

- No standard methodology for timing closure for on-chip IP communications
- Process node advances add to RC delays for long, cross-chip distances traveled
- Interconnects that connect different IP blocks span long distances and hence suffer from RC delays



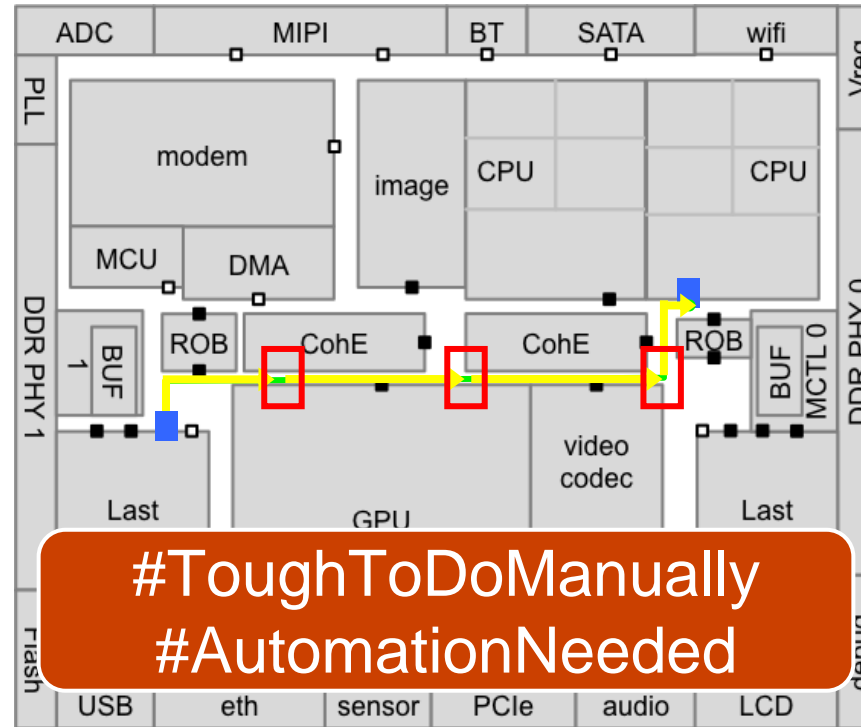
Source: Serkan Kincal, et al., "RC Performance Evaluation of Interconnect Architecture Options Beyond the 10-nm Logic Node," IEEE (2014)

Timing Issues: Can't Cross Advanced Node SoCs in One Clock Cycle

Physical distance impacts the number of pipeline stages



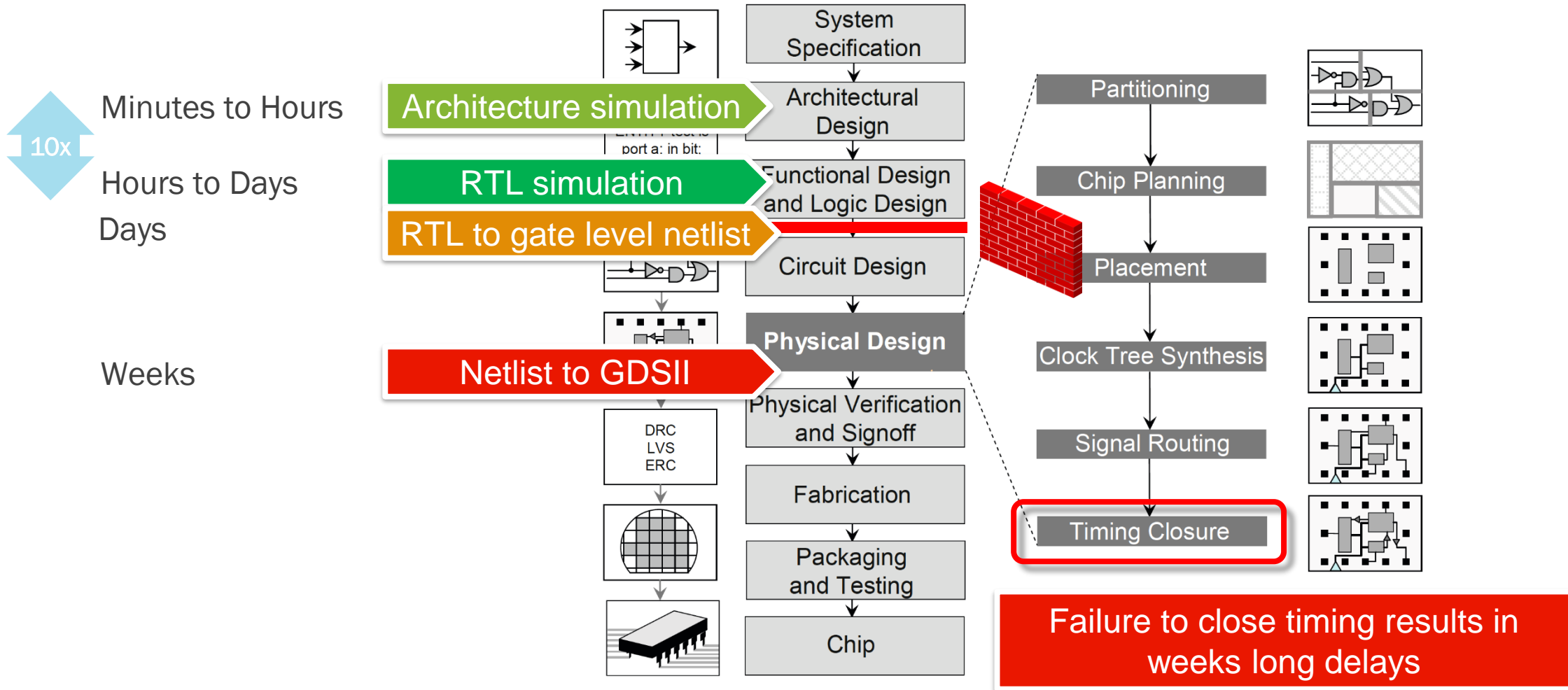
Clock Cycles



#ToughToDoManually
#AutomationNeeded

Transport delay = F (foundry, routing stack, type of driving cell, process voltage, temperature, ...)

The EDA Flow & NoC Design

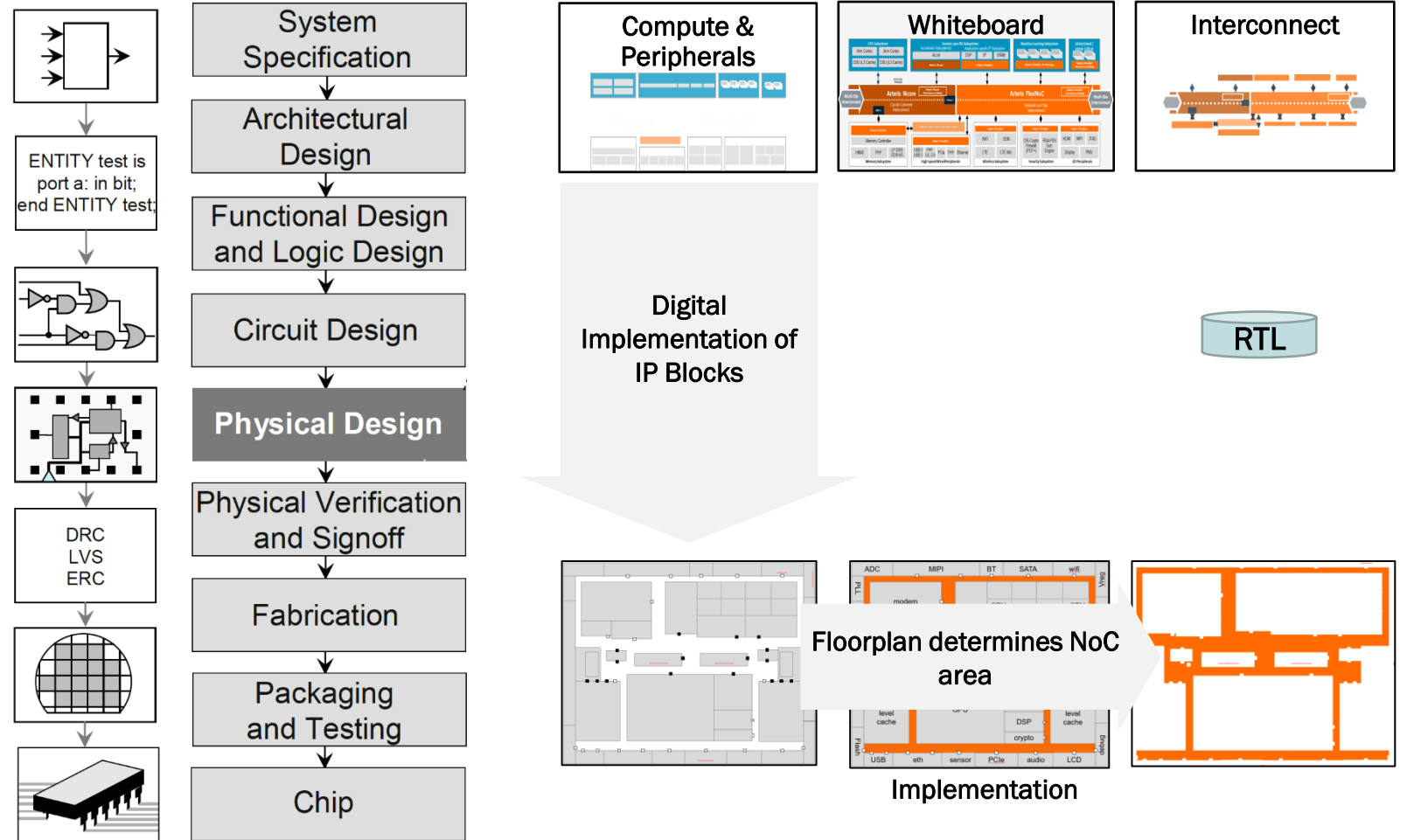


EDA flow diagram source: Andrew B. Kahng, et al., "VLSI Physical Design: From Graph Partitioning to Timing Closure," Springer (2011)

The EDA Flow & NoC Design

Customer uses Arteris tools to design the Network-on-Chip (NoC)

Customer uses EDA tools to implement from RTL to GDSII

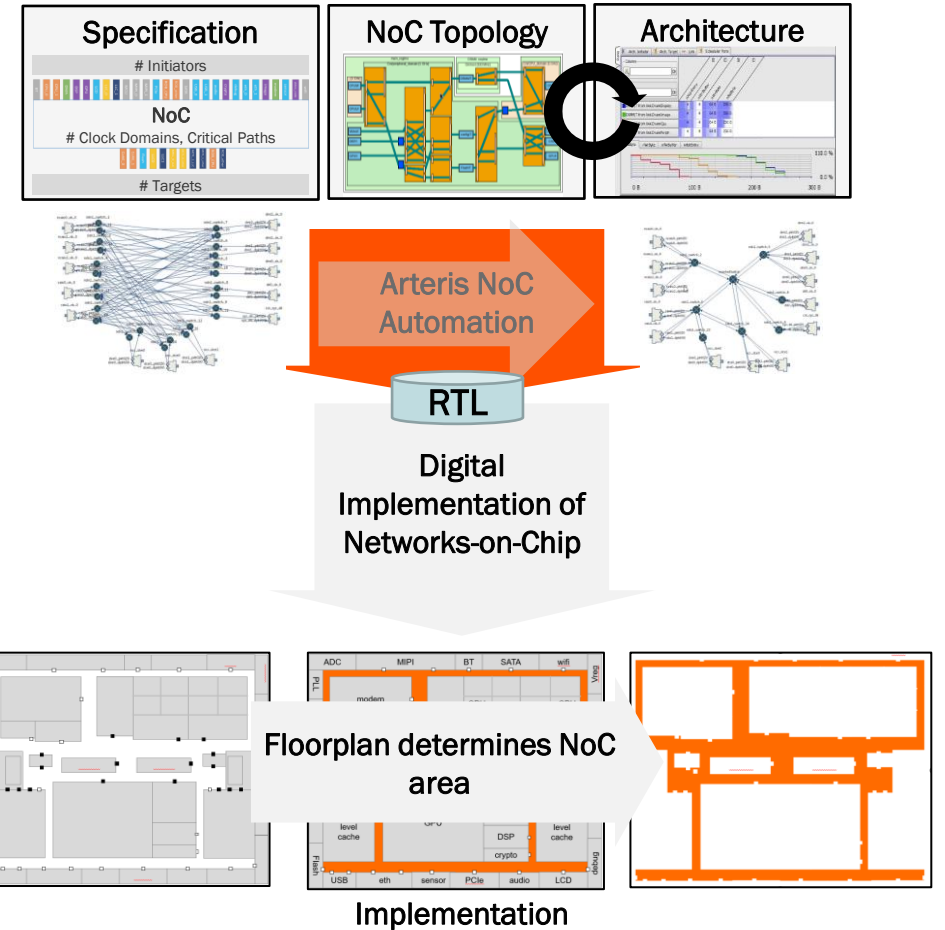
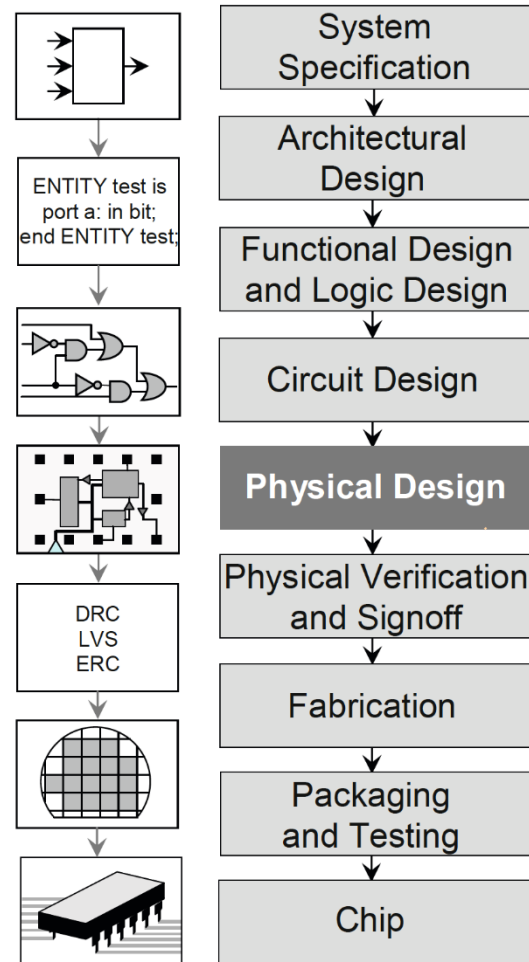


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FlexNoC 5 IP Development Flow

Inputs

Specification
Socket specifications

Floorplan outline
LEF/DEF
Visio

Perf Analysis
Traffic Scenarios

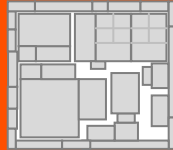
P&R
Timing Reports

Specification

Column	Row	Modifications	Defer	clock	bus type	power	width	depth	compression	data path
B Initiator	B CPU0	mainRegime/CmRoot	AXI Initiator	...	[x0]	...	Separated			
B CPU1	mainRegime/CmRoot	AXI Initiator	...	[x0]	...	Separated				
B DSP	mainRegime/CmRoot	AXI Initiator	...	[x0]	...	Separated				
B GPU	mainRegime/CmRoot	AXI Initiator	...	[x0]	...	Separated				
B Video	mainRegime/CmRoot	AXI Initiator	...	[x0]	...	Separated				
B Target	B DRAM	mainRegime/CmRoot	AXI Target	...	[x0]	...	Separated			
B Flash	mainRegime/CmRoot	AXI Target	...	[x0]	...	Separated				
B config	mainRegime/CmRoot	AXI Target	...	[x0]	...	Separated				

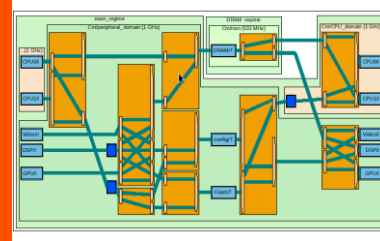
Physical Awareness &

auto pipe,
placement



Architecture

switch topology
QoS, buffers
serialization



Performance Analysis

use case
based
performance



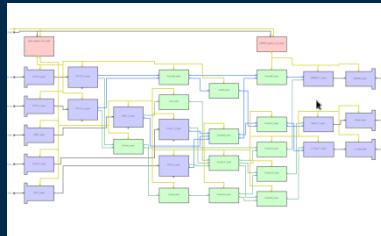
Outputs

Structure
RTL
SystemC
IP-XACT

Scripts /
constraints
Gate Estimates

Verification
testbenches

Structure



Timing
reports

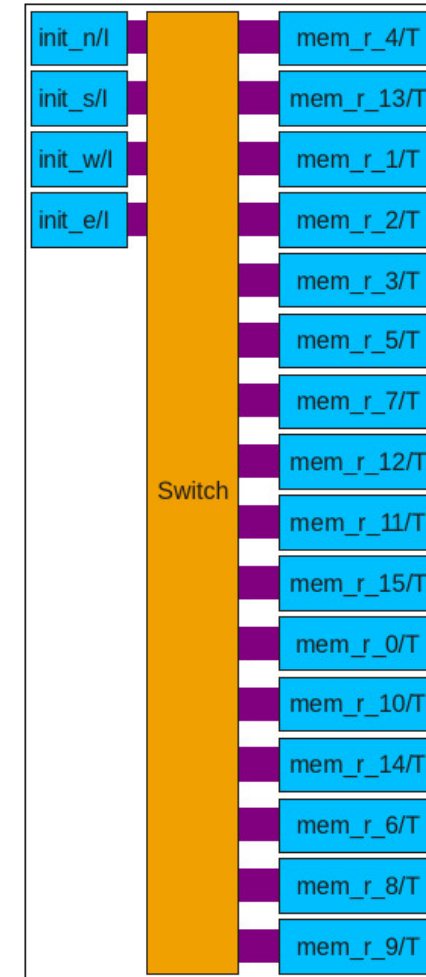
P&R

Synthesis

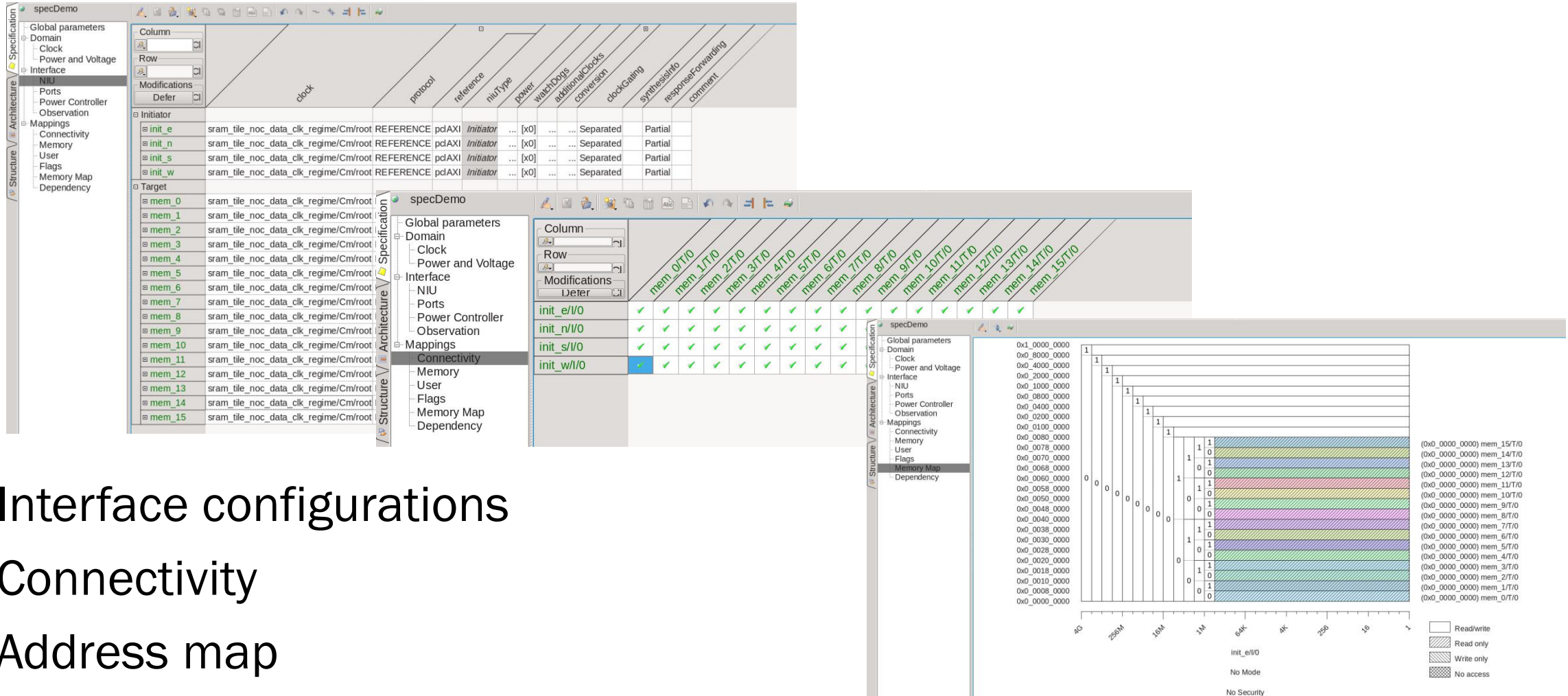
Timing reports
For visualization

Signal Processing Design Example

- The use case is signal processing as part of a larger Communications SoC
- The design includes x4 DMAs that need to access 'scratchpad' SRAMs
- A crossbar approach is a good starting point



NoC Specification Capture



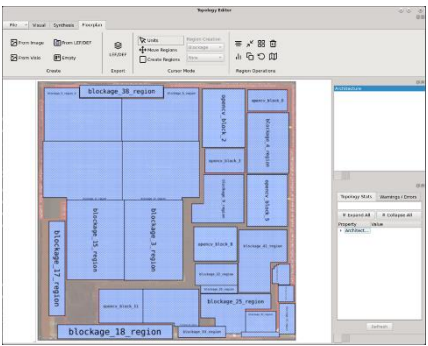
- Interface configurations
- Connectivity
- Address map

Floorplan Input

EARLY stage:
Image



Import



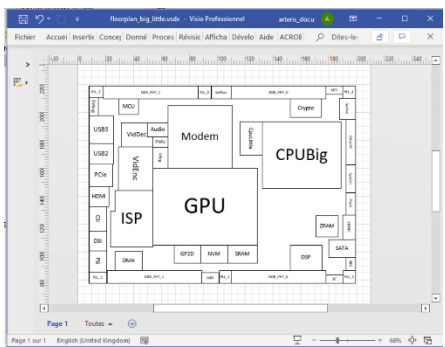
file
Tcl

Export

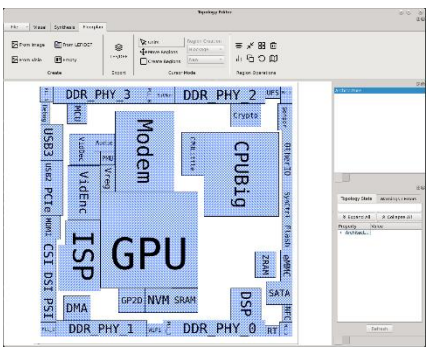
LEF/DEF



Visio



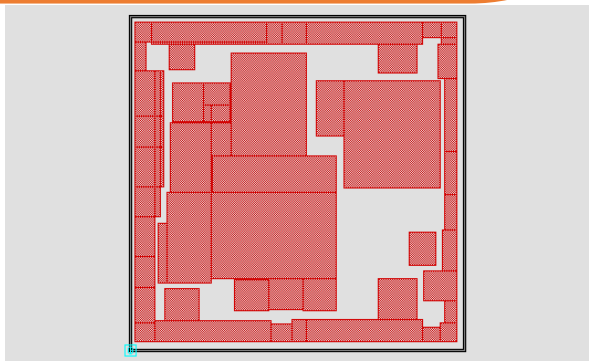
Import



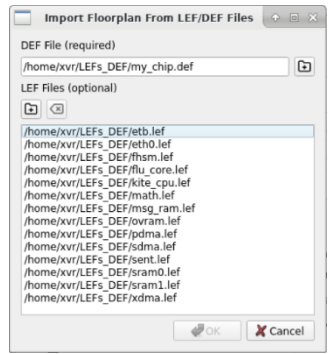
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TCL

Export

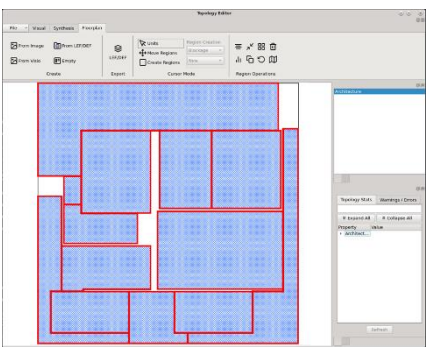
LEF/DEF



LATER stage:
LEF/DEF



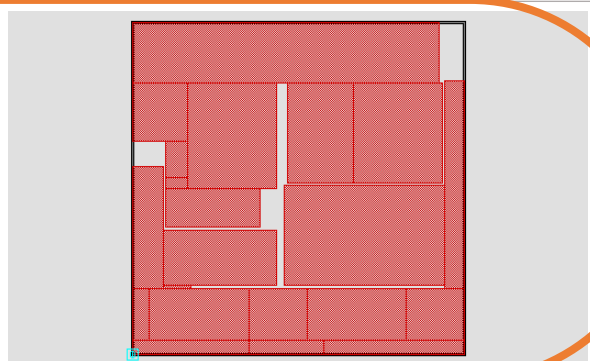
Import



file
Tcl

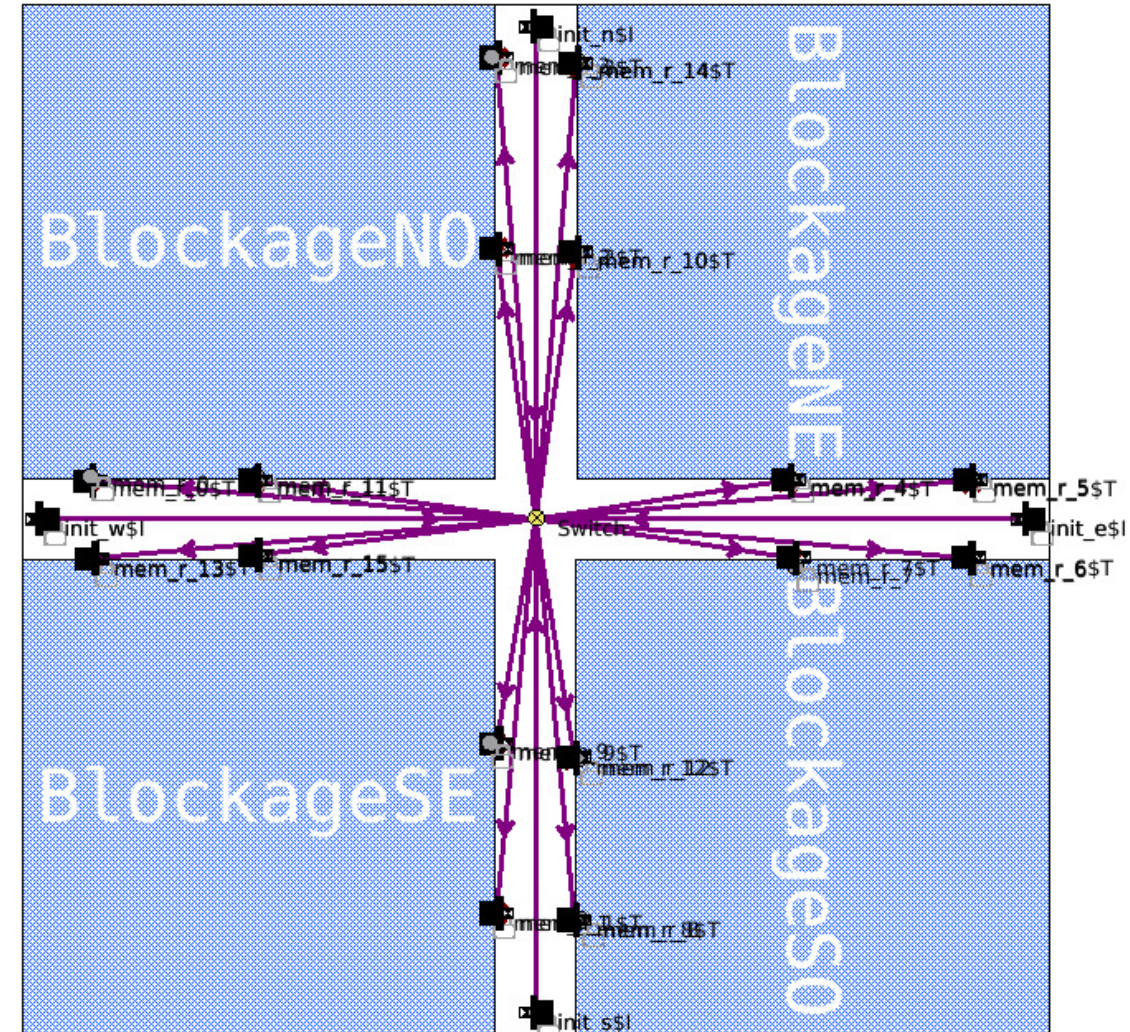
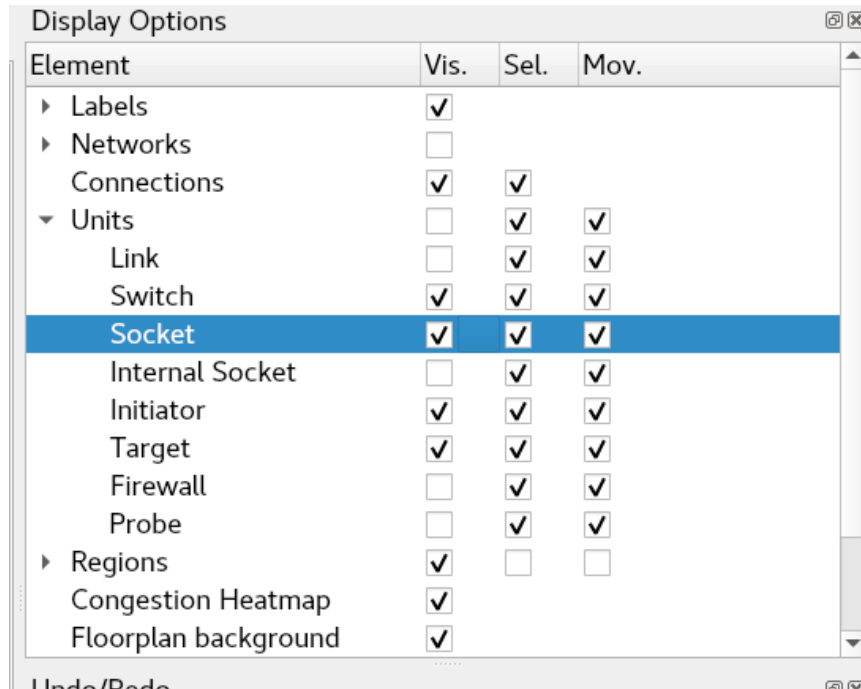
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LEF/DEF

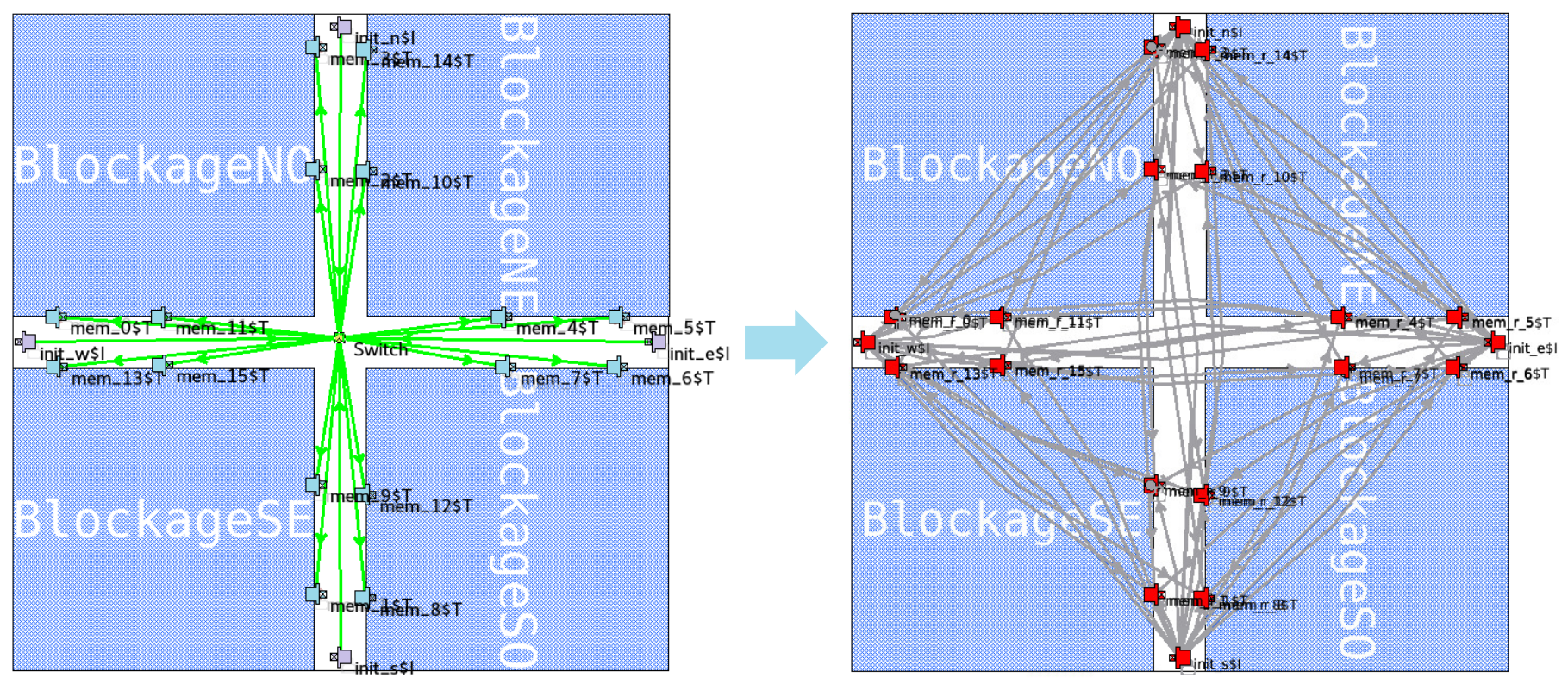


Initial NoC Topology

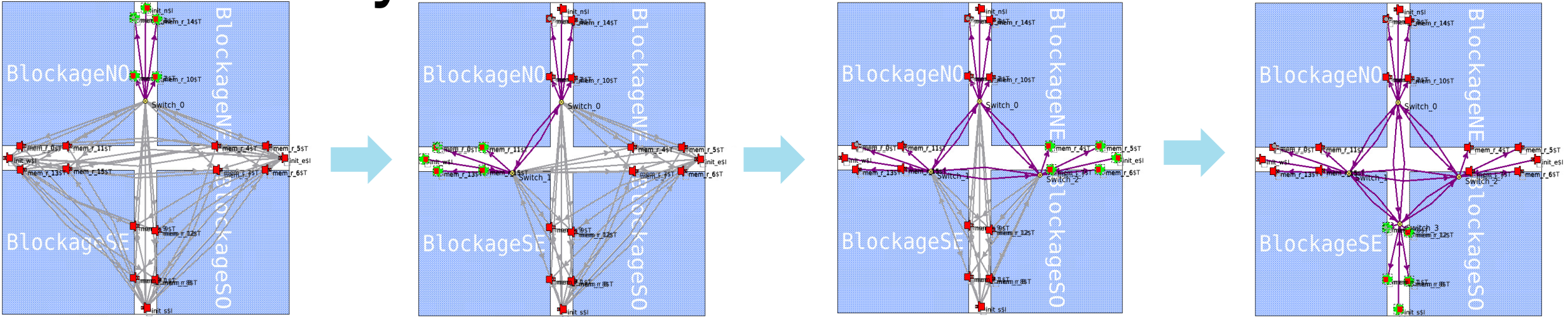
- FlexNoC will place the initial topology
 - This is a starting point
 - Note the possible central congestion issue



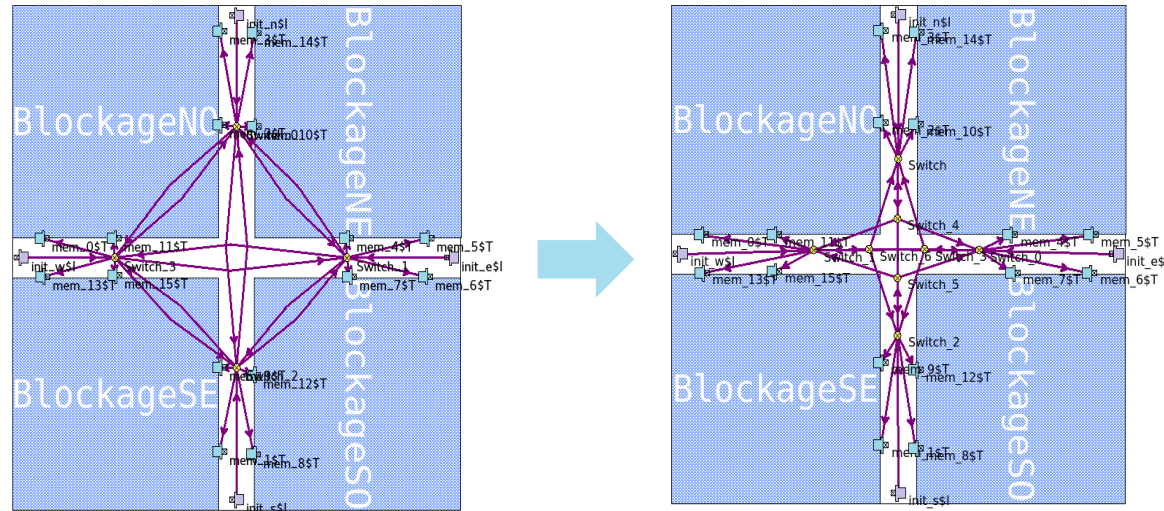
Initial NoC Topology is Reset



More Optimal Version Created using the Physical Layout View



- Switches are added
- And then smaller switches with fewer wires
- Design is optimized, and congestion is reduced.

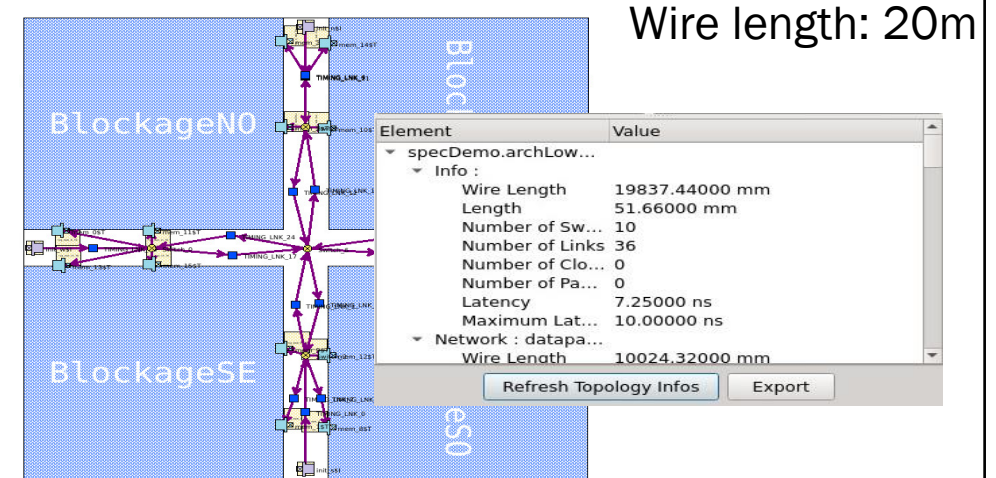
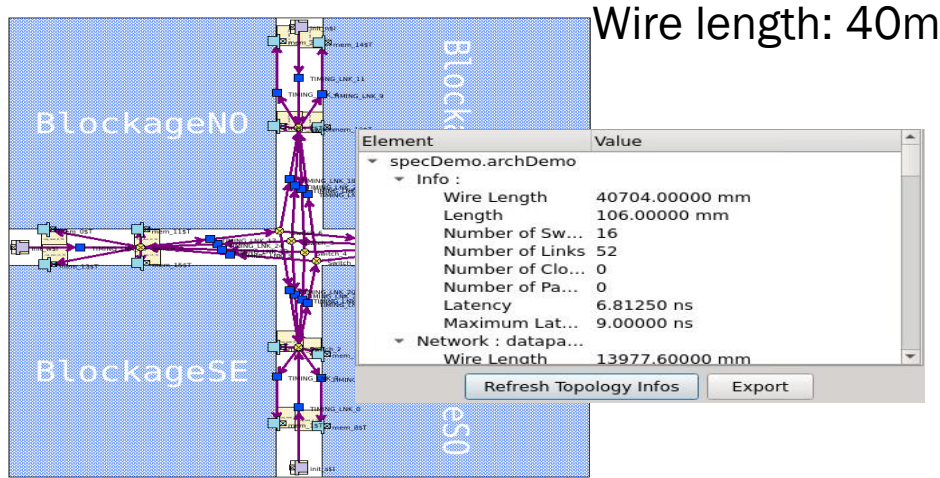


Design Optimization using Physical and Performance Co-design: 50% wire length reduction within performance goals

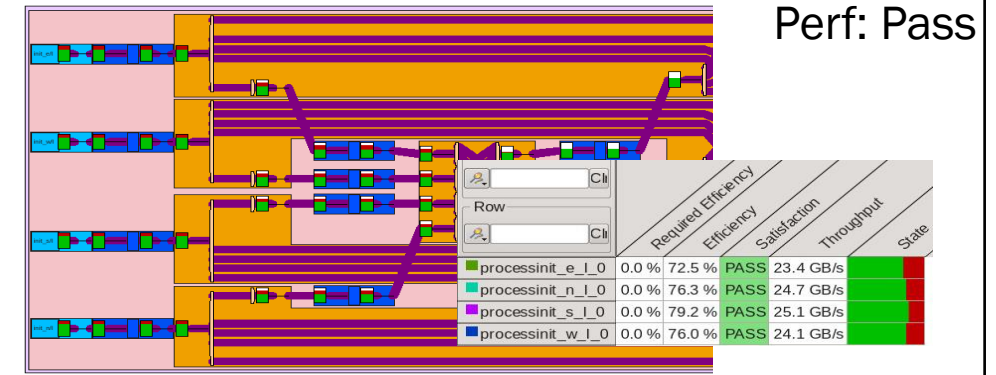
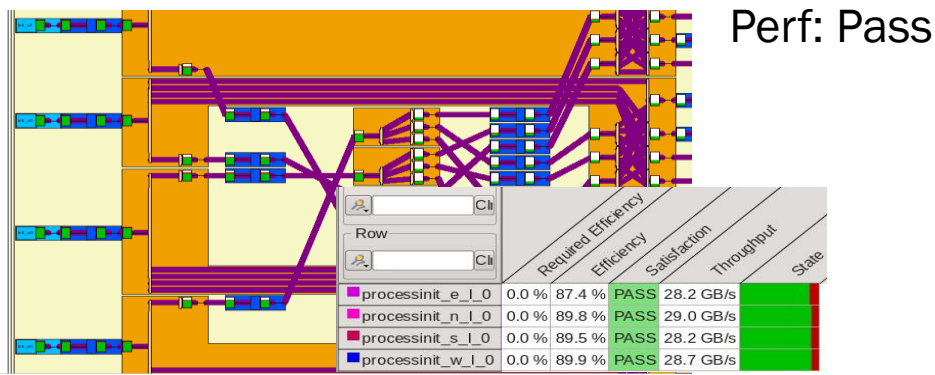
- Before

- After

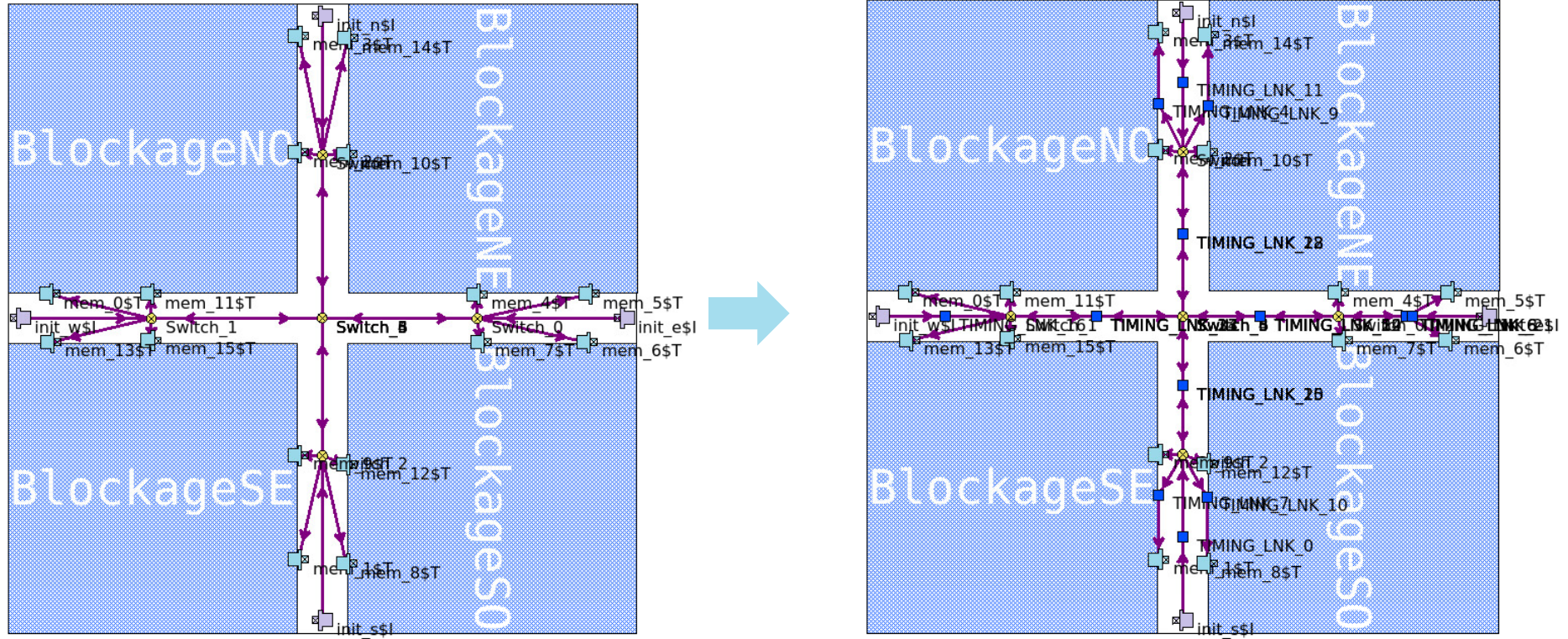
Physical
Design
View



Performance
Modelling
View

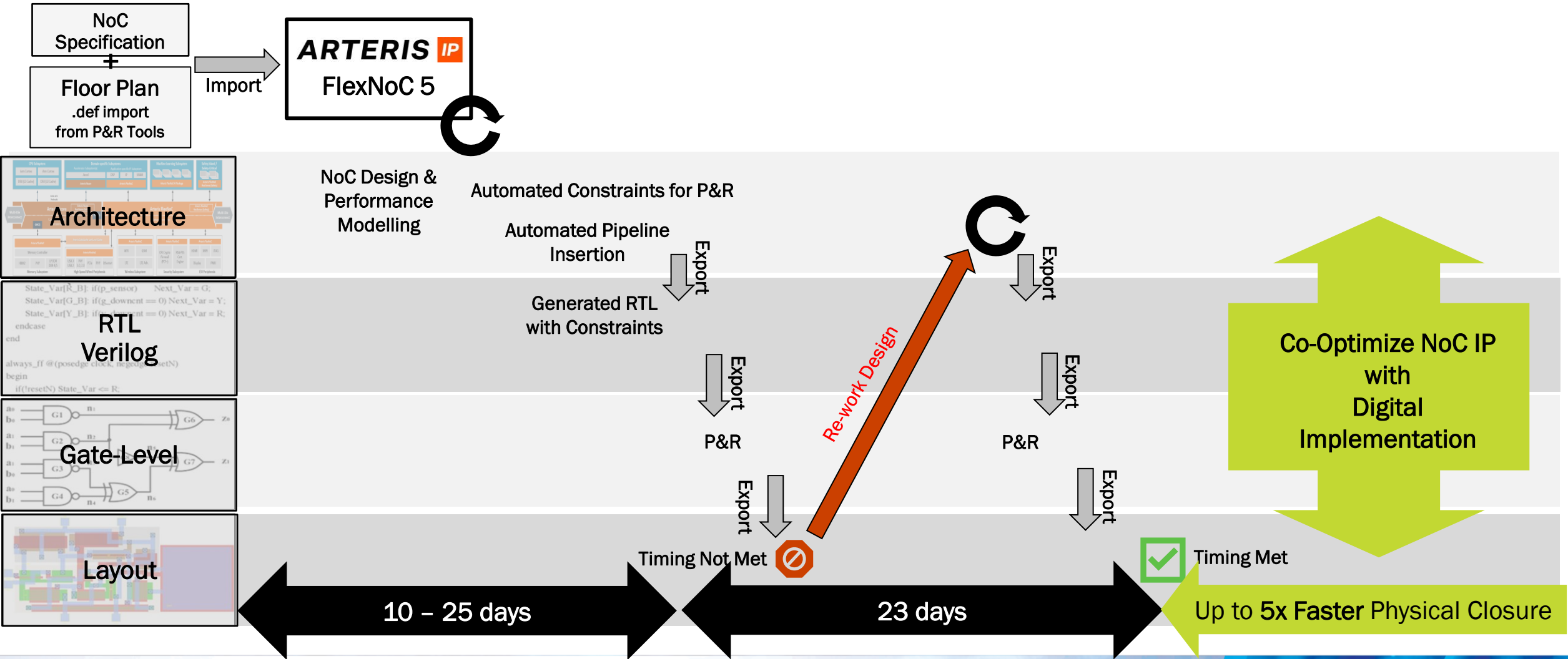


Pipeline Placeholders are Added to Assist Timing Closure



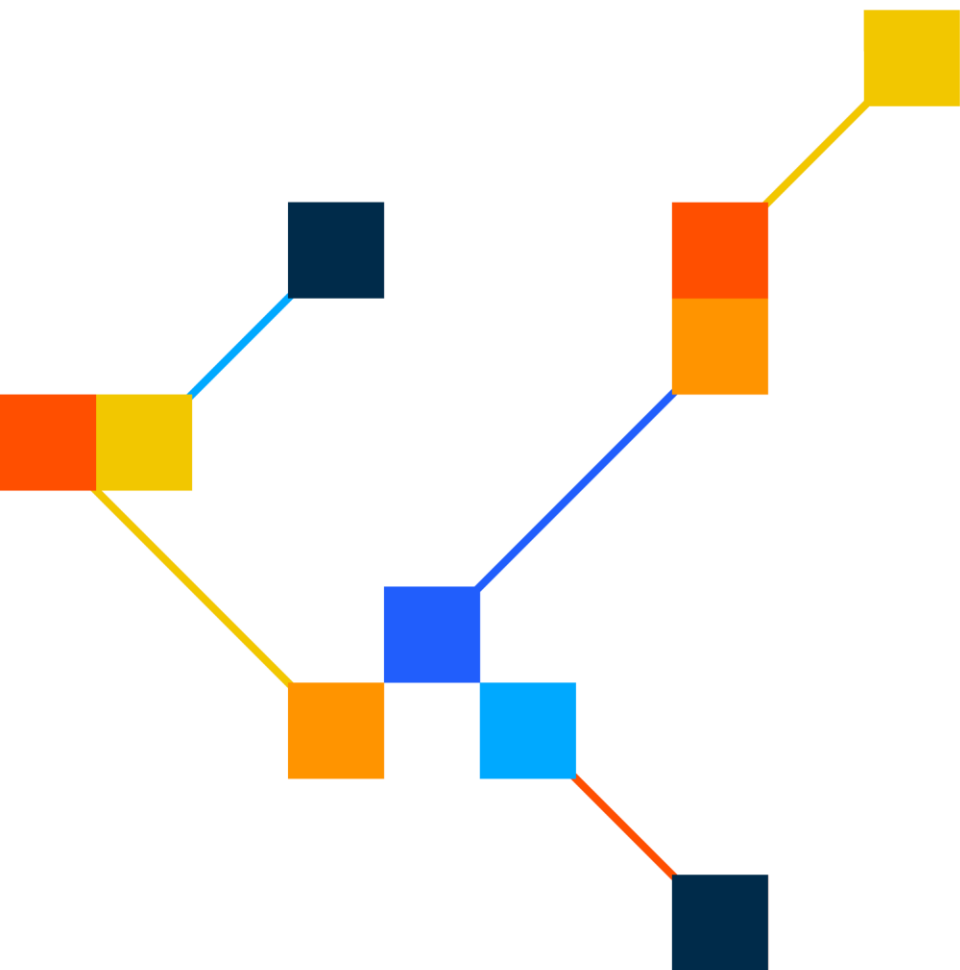
E.g. 1GHz design, 5mm², 1ns per mm propagation speed

Avoiding late timing issues using abstraction, physical awareness, and estimation



Summary

- The **number of IP blocks** in Systems-on-Chip and across chiplets **continues to grow**
- As a result, **Networks-on-Chip (NoCs)** with complex protocols like AMBA AXI, CHI, and many others **have emerged and continue to grow in complexity**
- The **floorplan** in digital implementation **determines the area that NoCs can consume**, and with a lack of a standard methodology for timing closure for on-chip IP communications, **timing closure** in layout **often requires a “return to the drawing board”** and a re-spin of the NoC architecture
- **Considering the floorplan information during the NoC architecture phase**, combined with early **estimation of pipeline stages** based on .lib technology information and **direct connection to digital implementation** using constraints, can significantly reduce the to physical closure
- This presentation introduces a methodology for **“Physically Aware NoC IP Development”**



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